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UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	TI-31026	Total Pages	21
	First Named Inventor or Application Identifier			
	Brodsky, et al.			
	Express Mail Label No.	EL591310799US		

APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.		ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
<p>1. <input checked="" type="checkbox"/> Fee Transmittal Form (Submit an original, and a duplicate for fee processing)</p> <p>2. <input checked="" type="checkbox"/> Specification [Total Pages 16] 1 (preferred arrangement set forth below)</p> <ul style="list-style-type: none">- Descriptive title of the invention- Cross References to Related Applications- Statement Regarding Fed sponsored R & D- Reference to Microfiche Appendix- Background of the invention- Brief Summary of the invention- Brief Description of the Drawings (if filed)- Detailed Description- Claim(s)- Abstract of the Disclosure <p>3. <input checked="" type="checkbox"/> Drawings(s) (35 USC 113) [Total Sheets 4] 1</p> <p>4. <input checked="" type="checkbox"/> Oath or Declaration [Total Pages 1] 1</p> <p>a. <input checked="" type="checkbox"/> Newly executed (original or copy)</p> <p>b. <input type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below]</p> <p>i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).</p> <p>5. <input type="checkbox"/> Incorporation by Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.</p>		<p>6. <input type="checkbox"/> Microfiche Computer Program (Appendix)</p> <p>7. <input type="checkbox"/> Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)</p> <p>a. <input type="checkbox"/> Computer Readable Copy</p> <p>b. <input type="checkbox"/> Paper Copy (identical to computer copy)</p> <p>c. <input type="checkbox"/> Statement verifying identity of above copies</p>	
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Complete if Known

Application Number **TBD**
Filing Date **Herewith**
First Named Inventor **Brodsky et al.**
Group Art Unit **TBD**
Examiner Name **TBD**
Attorney Docket Number **TI-31026**

TOTAL AMOUNT OF PAYMENT (\$) **\$880.00**

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to.

Deposit Acct. # **20-0668**

Deposit Acct. Name. **Texas Instruments, Inc.**

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and 1.17

☐ Charge the Issue Fee Set in
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FEE CALCULATION

1. FILING FEE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
101	690	201	345	Utility filing fee	690
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	760	208	380	Reissue filing fee	
114	150	214	75	Provisional fee	

SUBTOTAL (1) **\$ 690.00**

2. CLAIMS

Total Claims	Extra	Fee from below	Fee Paid
24	-20 = 4	X 18	X 72
Independent Claims	4	-3 = 1	X 78
Multiple Dependent Claims		X	X

Large Entity		Small Entity		Fee Description
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple Dependent claims
109	78	209	39	Reissue independent claims over original patent
110	18	210	9	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$) **\$150.00**

FEE CALCULATION (continued)

Large Entity		Small Entity		Fee Description
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
105	130	205	65	Surcharge-late filing fee or oath
127	50	227	25	Surcharge-late provisional filing fee or over sheet.
139	130	139	130	Non-English specification
147	2520	147	2520	For filing a request for reexamination
112	920	112	920	Requesting publication of SIR prior to Examiner action
113	1840	113	1840	Requesting publication of SIR after Examiner action
115	110	215	55	Extension for reply within first month
116	380	216	190	Extension for reply within second month
117	870	217	435	Extension for reply within third month
118	1360	218	680	Extension for reply within fourth month
128	1850	228	925	Extension for reply within fifth month
119	300	219	150	Notice of Appeal
120	300	220	150	Filing a brief in support of an appeal
121	260	221	130	Request for oral hearing
138	1510	138	1510	Petition to institute a public use proceeding
140	110	240	55	Petition to revive-unavoidable
141	1210	241	605	Petition to revive-unintentional
142	1210	242	605	Utility issue fee (or reissue)
143	430	243	215	Design issue fee
144	580	244	290	Plant issue fee
122	130	122	130	Petitions to the Commissioner
123	50	123	50	Petitions related to provisional applications
126	240	126	240	Submission of Information Disclosure Statement
581	40	581	40	Recording each patent assignment per property (x # of properties)
146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))

Other fee (specify) _____

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SUBMITTED BY

complete (if applicable)

Typed or Printed Name **Brian A. Carlson**

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Signature

Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: BRODSKY, et al.

Art Unit: TBD

Serial No.: TBD

Examiner: TBD

Filed: Herewith

Docket: TI-31026

For: Circuit and Method for An Integrated Charged Device Model Clamp

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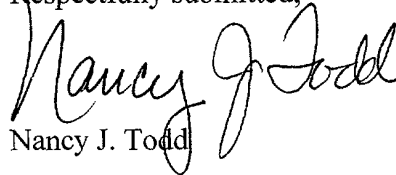
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- Utility Patent Application Transmittal (1 page)
- Complete Copy of Patent Application (20 pages), to include:
 - Specification (16 pages)
 - Drawings (4 pages)
- Declaration and Power of Attorney (1 page)
- Assignment Recordation Cover Sheet (1 page)
- Copy of Original Signed Assignment (1 page)
- Information Disclosure Statement and PTO-1449 form (2 pages)
 - Five (5) References
- Fee Transmittal (1 original and 1 copy)

Respectfully submitted,


Nancy J. Todd



09/25/00 09/25/00

CIRCUIT AND METHOD FOR AN INTEGRATED CHARGED DEVICE MODEL CLAMP

TECHNICAL FIELD

5 The present invention relates generally to integrated circuits, and more particularly to a circuit and method for an integrated charged device model clamp.

BACKGROUND

10 Integrated circuit ("IC") technology continues to improve, resulting in ICs with increasing density and devices with smaller and smaller geometries. As the devices become more miniaturized, however, they generally become more susceptible to electrostatic discharge ("ESD") damage. If ESD is not properly contained, it can lower a device's reliability or even destroy the device.

15 An ESD event typically occurs when an IC (e.g., a metal oxide semiconductor ("MOS") IC) is handled by a human being or by a machine. During an ESD event, a large voltage is applied to the IC. Generally, to avoid damage to the IC during an ESD event, ESD protection devices are typically fabricated on the IC and connected to the IC input/output pads and input/output circuits and other internal nodes of the IC. As used
20 herein with respect to a component in an IC, the phrase "input/output" means that the component is used for either input or output, or both. ESD protection devices generally provide discharge paths so that the internal circuits of the IC are not damaged during the ESD event.

25 Different ESD tests may be used to evaluate the effectiveness of ESD protection devices. Three ESD tests typically used include: the human body model ("HBM") test, a machine model ("MM") test and a charged device model ("CDM") test. Different ESD protection devices may be needed to optimize the level of ESD protection provided for the different ESD tests.

30 A detailed description of CDM events and IC design guidelines is provided in Timothy Maloney, "Designing MOS Inputs and Outputs to Avoid Oxide Failure in the Charged Device Model," EOS/ESD SYMPOSIUM PROCEEDINGS, 1988, pp. 220-27.

Generally, a CDM test simulates a charged device contacting a grounded surface (e.g., metal), typically associated with automated handling equipment in the production/manufacturing environment. A CDM test may be performed in the following manner. First, the device to be tested is charged. Most of this charge is stored in the VDD voltage supply rail and/or the ground supply rail within the device. Then one of the pads of the charged device is connected to an external ground. The charges stored in the VDD and/or ground supply rail then find pathways flowing to the pad under test, typically dissipating the charge within nanoseconds, thus testing the ESD protection devices implemented in the IC.

While primary ESD structures (e.g., PDNMOS, BTNMOS, dual-diodes) placed near the input/output pads of a device generally provide protection against HBM and MM events, they do not necessarily provide sufficient protection against CDM events. Generally, the most common damage caused by a CDM event is the rupture of thin dielectrics in the IC, such as MOS gate dielectrics or capacitor dielectrics. CDM clamps are therefore used to provide protection of internal IC input circuits against charged device ESD events. Generally, in prior art circuits, the CDM clamp devices are separated from the internal input circuit transistors, with a metal interconnect system providing the connections between the CDM clamps and the input circuit.

A disadvantage of the prior art circuits is that the metal/contact/via physical characteristics of this metal interconnect system may significantly increase the parasitic resistance and inductance of the circuit. Generally, in order for CDM clamps to be effective, the parasitic resistance and inductance between the ground/power-supply connections of the internal input circuit and the ground/power-supply connections of the CDM clamps must be minimized. Because the input circuitry may not reside in close physical proximity to its CDM ESD protection structure, however, there may be significant parasitic resistance and inductance in the metal ground bus between the CDM ESD structure and the input circuit inverter/buffer.

Generally, the parasitic inductance and resistance between the ground connection of the CDM clamp and the ground connection of the input circuit act in series with the clamp voltage of the CDM clamp, building up excess voltage across the pin being protected and ground. Likewise, the parasitic inductance and resistance between

SUMMARY OF THE INVENTION

These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention in which a CDM clamp circuit is integrated into the interface circuit being protected on the IC. Generally, the integrated CDM clamp circuit and interface circuit are adjacent to each other and share a common device element or component, thus eliminating the need for a metal interconnect. Because there is no interconnect, the parasitic resistance and inductance are also minimized or eliminated from the circuit, thus reducing or eliminating the excessive voltage drop present in prior art circuits.

Preferably, the CDM clamp circuit is integrated into the circuit that it is protecting by having the two circuits share the same silicon source region. In a preferred embodiment input circuit, the same diffusion region is the source of both the input transistor and its associated CDM clamp transistor. In one preferred embodiment, a PMOS input transistor and a PMOS CDM clamp transistor share a single p+ diffusion region. In another preferred embodiment, an NMOS input transistor and a NMOS CDM clamp transistor share a single n+ diffusion region.

An advantage of a preferred embodiment of the present invention is that it generally eliminates the need for a metal interconnect between the sources of the CDM clamp device and the internal circuit device.

Another advantage of a preferred embodiment of the present invention is that, by eliminating the source metal interconnect, it generally minimizes or eliminates parasitic resistance and inductance between the ground/power-supply connection of the internal input circuitry and the ground/power-supply connection of the CDM clamp device.

Another advantage of a preferred embodiment of the present invention is that it reduces the area on the IC needed for CDM protection because the devices are located directly adjacent to each other and because each CDM clamp shares a source region with the transistor that it is protecting.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be

described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also
5 be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

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BRIEF DESCRIPTION OF THE DRAWING

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

FIGURE 1 is a schematic of an IC input circuit with CDM clamps;

FIGURE 2 is a schematic of a transistor implementation of a diode-to-ground CDM clamp;

FIGURE 3A is a cross-sectional view of a diode-to-supply CDM clamp;

FIGURE 3B is a schematic of a transistor implementation of a diode-to-supply CDM clamp;

FIGURE 4A is a schematic of an IC input circuit with MOS transistor CDM clamps;

FIGURE 4B is a plan view of an IC input circuit with integrated CDM clamps; and

FIGURE 4C is a cross-sectional view of an IC input circuit with integrated CDM clamps.

DETAILED DESCRIPTION

The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

The present invention will be described with respect to preferred embodiments in a specific context, namely an IC input circuit comprising PMOS and NMOS input transistors, with PMOS and NMOS CDM clamp transistors sharing the source diffusion regions of the respective input transistors. Preferred embodiments of the invention may be applied, however, to other integrated ESD and interface circuits. For example, the preferred embodiments may be applied to MOS, CMOS or BiCMOS ICs. Preferred embodiments may be applied to other field effect devices or to advanced bipolar technologies. In addition, preferred embodiments may be used to protect other IC interface circuits connected to the pads of the IC, such as input/output ("I/O") circuits or output circuits.

With reference now to Fig. 1, there is shown a schematic of a CDM protection scheme for an IC MOS input circuit. The input circuit comprises PMOS input transistor 102 and NMOS input transistor 104. Output 108 is connected to other internal IC circuitry. CDM clamp diodes 114 and 116 are connected to input transistors 102 and 104, respectively, to provide protection against CDM events. Input 106 is connected to IC input pad 110 via input resistor 112. Input resistor 112 is chosen so as to limit the current in the CDM clamps, and typically has a value of about 200-400 ohms, although it may be higher or lower than those values.

As shown in Fig. 2, CDM clamp diode 116 between nodes A and B may be implemented as grounded-gate NMOS device 202. As shown in Fig. 3A, CDM clamp diode 114 between nodes A and C may be implemented as a standard PN diode 302 with anode 304 formed by a boron implant in n-type well 306. n+ region 308 provides a contact to n-well 306, which forms the cathode of the diode. Alternatively, CDM clamp

diode 114 may be implemented as PMOS device 310 with its gate connected to the power supply voltage.

Referring back to Fig. 1, and as discussed hereinabove, ESD event 118 connects input pad 110 to ground, discharging any charge stored in the VDD and/or ground supply rails of the IC through input pad 110. Preferably, the parasitic resistance between a CDM clamp and its respective input transistor should generally be kept below 0.5 ohms. In the prior art, however, because the CDM clamps and the input transistors are not integrated, metal interconnects are used to connect the devices. These metal interconnects create parasitic resistance and inductance R^* 120 and 122 between the CDM clamps and their input transistors, thus interfering with the proper operation of the CDM protection mechanism.

In a preferred embodiment of the present invention, because both of the CDM clamping diodes may be implemented using MOS devices, the CDM clamps may be integrated into the input transistors, as shown in Fig. 4. By integrating the CDM clamps into the same active area as the input transistors of the internal input circuit, the parasitic resistance and inductance are minimized between the ground/power-supply connections of the CDM clamps and the input transistors. Fig 4A illustrates integrated CDM clamp/input circuit 400 in schematic form. Fig. 4B illustrates a top down view of circuit 400 as implemented in a semiconductor substrate, while Fig. 4C illustrates a cross-section of circuit 400 as implemented in a semiconductor substrate. Note that input resistor 410 in Fig. 4A is not shown in Figs. 4B and 4C. Ground node 402, input node 404, output node 406 and power supply node 408 are the same in each of the Figures 4A, 4B and 4C.

In Figs. 4B and 4C, the NMOS devices are formed in p-substrate 420, and the PMOS devices are formed in n-well 422. PMOS input transistor 412 in Fig. 4A comprises p+ drain 434, polysilicon gate 432, and p+ source 430 in Figs. 4B and 4C. NMOS input transistor 414 in Fig. 4A comprises n+ drain 436, polysilicon gate 438, and n+ source 440 in Figs. 4B and 4C. CDM clamp PMOS transistor 416 in Fig. 4A comprises p+ drain 426, polysilicon gate 428, and p+ source 430 in Figs. 4B and 4C. CDM clamp NMOS transistor 418 in Fig. 4A comprises n+ drain 444, polysilicon gate 442, and n+ source 440 in Figs. 4B and 4C. Of course, each of the above devices also

comprises a gate dielectric and channel underlying the gate. Contact to p-substrate 420 is provided by p+ contact 446, and contact to n-well 422 is provided by n+ contact 424.

As can be seen in Figs. 4B and 4C, PMOS input transistor 412 and CDM clamp PMOS transistor 416 share p+ source region 430 as a single source for both devices.

5 Similarly, NMOS input transistor 414 and CDM clamp NMOS transistor 418 share n+ source region 440 as a single source for both devices. A metal interconnect layer is not needed to connect the source regions of the devices, thus avoiding the parasitic resistance and inductance created by the metal interconnect of prior art devices.

10 Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, the specific transistor implementation of the inventive circuits may be varied from the examples provided herein while still remaining within the scope of the present invention. The layout and cross-section representations of the preferred embodiments are generic, and variations of the specific implementations
15 shown are within the scope of the present invention. As other examples, p-type and n-type semiconductor regions may be switched, or the source and drain of a MOS transistor may be switched. Devices may share a different common element other than the source. Integrated circuit materials other than those disclosed herein may be used.
20 As another alternative, multiple transistors or other devices such as diodes may be used for the CDM clamps or input transistors, or combinations may be used. As another alternative, there may be one clamp protecting an internal circuit, or more than two clamps protecting an internal circuit. The CDM clamps may be used in conjunction with other ESD protection devices.

25 Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently
30 existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may

be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

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WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

an input/output (I/O) pad;

an interface circuit connected to said I/O pad; and

a charged device model (CDM) clamp circuit connected to said pad and to said interface circuit, wherein said CDM clamp circuit and said interface circuit are adjacent to each other and share a common device element.

2. The integrated circuit of claim 1, further comprising a resistor disposed between said I/O pad and said interface circuit.

3. The integrated circuit of claim 1, wherein said CDM clamp circuit comprises a first transistor and said interface circuit comprises a second transistor.

4. The integrated circuit of claim 3, wherein said first and second transistors are MOS transistors.

5. The integrated circuit of claim 4, wherein said CDM clamp circuit and said interface circuit share a common source region.

6. The integrated circuit of claim 1, wherein said I/O pad is an input pad and said interface circuit is an input circuit.

7. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first PMOS transistor and said interface circuit comprises a second PMOS transistor, and wherein said common device element is a p+ source region.

8. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first NMOS transistor and said interface circuit comprises a second NMOS transistor, and wherein said common device element is an n+ source region.

9. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first PMOS transistor and a first NMOS transistor, wherein said interface circuit comprises a second PMOS transistor and a second NMOS transistor, wherein said first and second PMOS transistors share a p+ source region, and wherein said first and second NMOS transistors share an n+ source region.

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10. A method of protecting an integrated circuit from electrostatic discharge (ESD), said integrated circuit comprising an input/output (I/O) pad and an interface circuit connected to said I/O pad, said method comprising:

disposing a charged device model (CDM) clamp circuit adjacent to said interface circuit and connected to said pad and to said interface circuit; and
sharing a common device element between both said CDM clamp circuit and said interface circuit.

11. The method of claim 10, wherein said CDM clamp circuit comprises a first MOS transistor and said interface circuit comprises a second MOS transistor.

12. The method of claim 11, wherein said common device element is a source region.

13. The method of claim 10, wherein said I/O pad is an input pad and said interface circuit is an input circuit.

14. The method of claim 13, wherein said CDM clamp circuit comprises a first PMOS transistor and said interface circuit comprises a second PMOS transistor, and wherein said common device element is a p+ source region.

15. The method of claim 13, wherein said CDM clamp circuit comprises a first NMOS transistor and said interface circuit comprises a second NMOS transistor, and wherein said common device element is an n+ source region.

16. The method of claim 13, wherein said CDM clamp circuit comprises a first PMOS transistor and a first NMOS transistor, wherein said interface circuit comprises a second PMOS transistor and a second NMOS transistor, wherein said first and second PMOS transistors share a p+ source region, and wherein said first and second NMOS transistors share an n+ source region.

17. An integrated circuit comprising:

a semiconductor substrate;

a first drain region disposed in said substrate;

a first channel region disposed in said substrate directly adjacent to said first

5 drain region;

a first gate dielectric overlying said first channel region;

a first gate overlying said first gate dielectric;

a first source region disposed in said substrate directly adjacent to said first
channel region;

10 a second channel region disposed in said substrate directly adjacent to said first
source region and on a side of said first source region opposite to said first channel
region;

a second gate dielectric overlying said second channel region;

a second gate overlying said second gate dielectric; and

15 a second drain region disposed in said substrate directly adjacent to said second
channel region.

18. The integrated circuit of claim 17, further comprising an input/output pad
electrically coupled to said first gate and to said second drain region.

19. The integrated circuit of claim 17, wherein said substrate is p-type, and
wherein said source and drain regions are n+ regions.

20. The integrated circuit of claim 17, further comprising an n-well disposed in
25 said substrate around said regions, wherein said substrate is p-type, and wherein said
source and drain regions are p+ regions.

21. A method of forming an integrated circuit, said method comprising:
forming a first drain region in a semiconductor substrate;
forming a first source region in said substrate separated from said first drain
region solely by a first channel region;
5 forming a second drain region in said substrate separated from said first source
region solely by a second channel region, wherein said second channel region is a
different region than said first channel region;
forming a first gate dielectric overlying said first channel region and a second
gate dielectric overlying said second channel region; and
10 forming a first gate overlying said first gate dielectric and a second gate overlying
said second gate dielectric.

22. The method of claim 21, further comprising forming an input/output pad on
said semiconductor substrate electrically coupled to said first gate and to said second
15 drain region.

23. The method of claim 21, wherein said substrate is p-type, and wherein said
source and drain regions are n+ regions.

20 24. The method of claim 21, further comprising forming said source and drain
regions in an n-well in said substrate, wherein said substrate is p-type, and wherein said
source and drain regions are p+ regions.

CIRCUIT AND METHOD FOR AN INTEGRATED CHARGED DEVICE MODEL CLAMP

ABSTRACT OF THE DISCLOSURE

5 A CDM clamp circuit integrated into the interface circuit it is protecting on an integrated circuit. Generally, the integrated CDM clamp circuit and interface circuit are adjacent to each other and share a common device element or component, thus eliminating the need for a metal interconnect. Because there is no interconnect, the parasitic resistance and inductance are also minimized or eliminated from the circuit,
10 thus reducing or eliminating excessive voltage drop. Preferably, the CDM clamp circuit is integrated into the circuit that it is protecting by having the two circuits share the same silicon source region. In a preferred embodiment input circuit, the same diffusion region is the source of both the input transistor and its associated CDM clamp transistor.

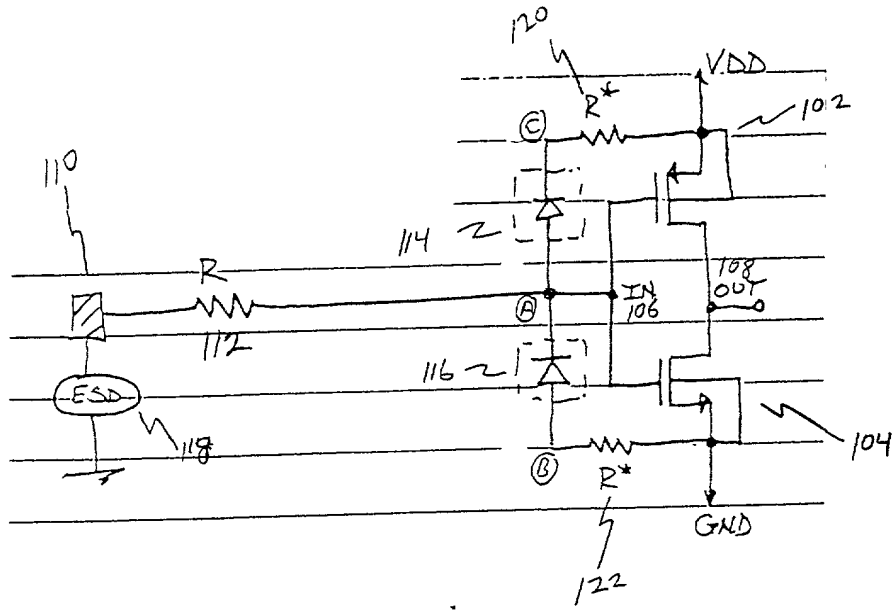


FIG. 1

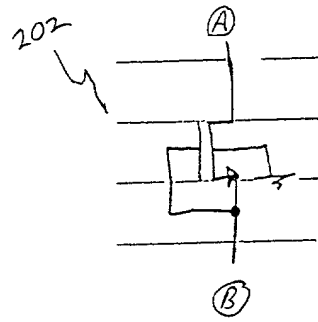


FIG. 2

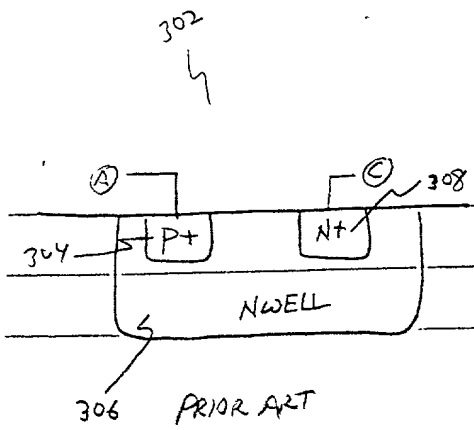


FIG. 3A

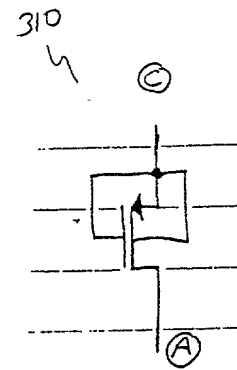


FIG. 3B

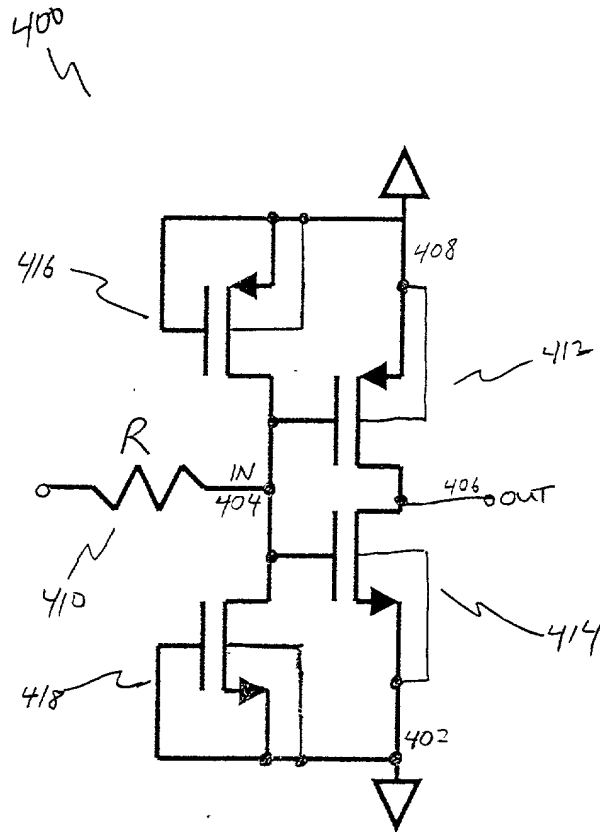


FIG. 4A

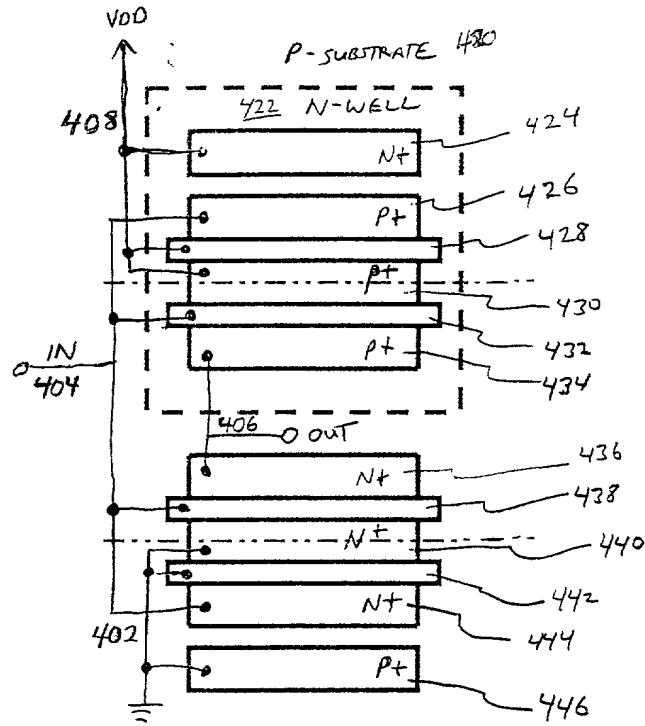


FIG. 4B

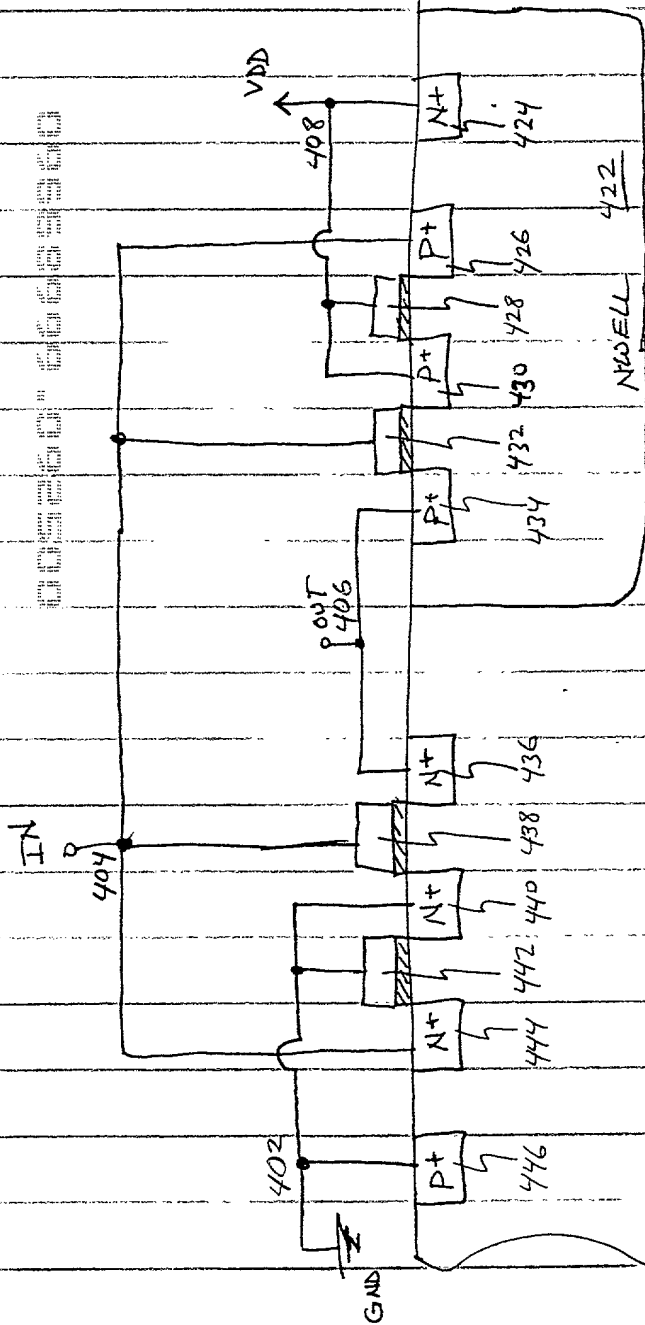
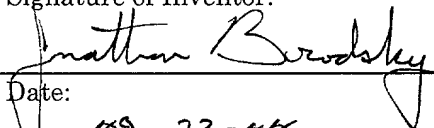
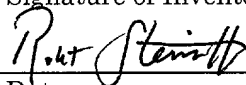
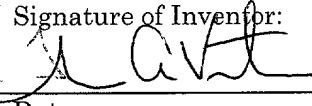


Fig. 4c

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:		
Circuit and Method for An Integrated Charged Device Model Clamp		
POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH.		
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Signature of Inventor: 	Signature of Inventor: 	Signature of Inventor: 
Date: 09-22-00	Date: 9/22/00	Date: 9-22-00